Notice of Allowability	Application No.	Applicant(s)	
	10/609,068	CAMERON, ANDREW JAMES	
	Examiner	Art Unit	
	Samir M. Shah	2856	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/25/2006*.

2. ☒ The allowed claim(s) is/are *1-3,5-8,10-16 and 18-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Samir M. Shah

ALLOWANCE

1. Claims 1-3, 5-8, 10-16 and 18-20 are allowed.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

(a) As to claims 1, 8 and 14, note is made of the limitations "adding the area occupied by the material in each grid element...to obtain a sum area", and "determining an average of the sum area over all grid elements" in combination with the rest of the limitations in the claims. Note is also made of the benefit of "adding the area occupied by the material in each grid element...to obtain a sum area", and "determining an average of the sum area over all grid elements" in the Specification (see paragraph 0007, lines 6-14; paragraph 0008).

(b) As to claims 1 and 8, the closest reference, Kim et al. (US Patent 6,484,300 B1 henceforth "Kim") discloses "a method of obtaining an effective pattern density" in an "integrated circuit"/determining the density variations of a material on multi-layer wafer including the steps of: "defining a grid of pattern cells" on each layer stacked on a wafer (column 7, lines 24-40, 61-67; column 8, lines 1-16; column 15, lines 10-13); determining a pattern density or the amount of metal within a given area in each grid element, each grid element having unique grid system co-ordinates (figure 4) and thereby computing a measure of the pattern density from the area of the material/metal in grid elements/pattern cells/windows in at least two of the layers stacked on a wafer (figure 4; column 3, lines 43-45, column 7, lines 22-40, 61-67; column 8, lines 1-16) (for

a detailed description of "pattern density" please refer to US Patent 5,552,996 to Hoffman et al.). Kim also discloses that a relative height difference in a patterned layer of an integrated circuit may degrade the operating characteristics of the integrated circuit and thus, prove to be a defect (column 1, lines 32-41); therefore, Kim discloses predicting a defect in the integrated circuit by detecting such a height difference on a layer of an integrated circuit, through the measure of the pattern density.

(c) As to claim 14, Kim discloses "a system for obtaining an effective pattern density" in an "integrated circuit"/for determining the density variations of a material on a multi-layer wafer including: "means for defining a grid of pattern cells" on a layer of an integrated circuit/each layer stacked on a wafer (column 7, lines 24-40, 61-67; column 8, lines 1-16; column 17, lines 18-22); means for determining a pattern density or the amount of material/metal within a given area in each grid element/pattern cell/window, of the grid system, on each of the layers stacked on a wafer (figure 4; column 3, lines 43-45, column 7, lines 22-40, 61-67; column 8, lines 1-16) (for a detailed description of "pattern density" please refer to US Patent 5,552,996 to Hoffman et al.) and means for computing a measure of the pattern density from the area of the material/metal in grid elements/pattern cells/windows in at least two layers of the multi-layer (figure 4; column 3, lines 43-45, column 7, lines 22-40, 61-67; column 8, lines 1-16; column 17, lines 23-25).

(d) However, Kim fails to disclose, "in at least two layers in the multi-layer printed circuit board", "adding the area occupied by the material in each grid element...to obtain a sum area", and "determining an average of the sum area over all grid elements".

(e) Therefore, the prior art neither teaches nor provides a motivation to combine the above-mentioned limitations in combination with rest of the limitations in the claims 1, 8 and 14.

Conclusion

3. The prior art made of record and not relied upon, cited in the attached 892 form, is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samir M. Shah whose telephone number is (571) 272-2671. The examiner can normally be reached on Monday-Friday 9:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hezron Williams can be reached on (571) 272-2208. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Samir M. Shah
Art Unit 2856
9/8/2006

HEZRON WILLIAMS
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